
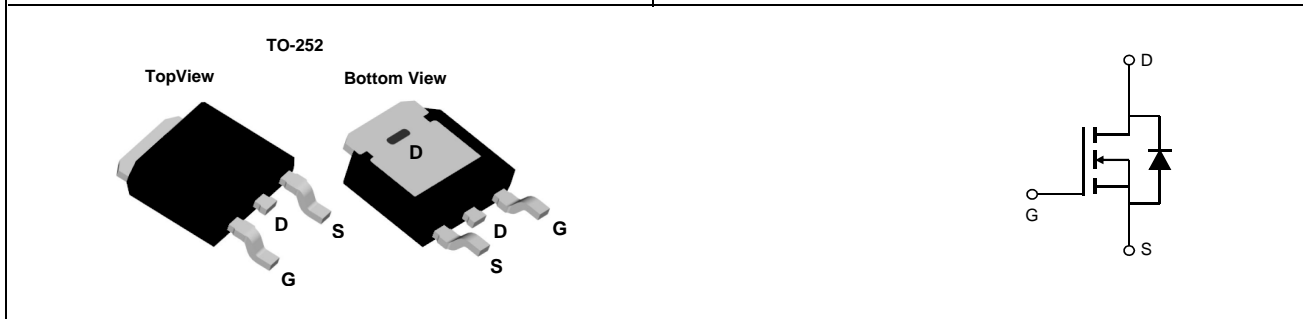


## TMD30N06D

### N-CHANNEL ENHANCEMENT MOSFET

<p><b>General Description</b></p> <p>The TMD30N06D uses advanced trench technology and design to provide excellent <math>R_{DS(ON)}</math> with low gate charge. It can be used in a wide variety of applications.</p>	<p><b>Product Summary</b></p> <p><math>V_{DS} = 60V, I_D = 30A</math>  <math>R_{DS(ON)} &lt; 27m\Omega @ V_{GS} = 10V</math></p> <p>100% UIS Tested              100% <math>R_g</math> Tested</p> <div style="text-align: right;">  </div>
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<b>Absolute Maximum Ratings (<math>T_c = 25^\circ C</math> unless otherwise noted)</b>			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	30	A
Drain Current-Continuous( $T_c = 100^\circ C$ )	$I_D(100^\circ C)$	20	A
Pulsed Drain Current	$I_{DM}$	74	A
Maximum Power Dissipation	$P_D$	50	W
Derating factor		0.33	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	144	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$
Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	3	$^\circ C/W$

## Electrical Characteristics (T<sub>c</sub>=25°C unless otherwise noted)

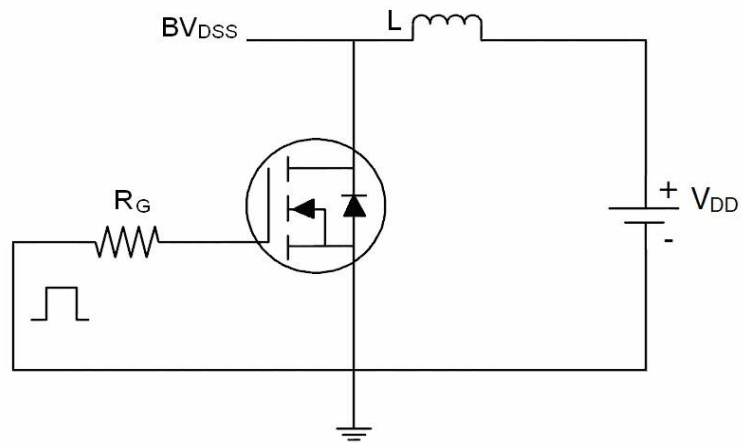
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.4	1.8	2.5	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	23	27	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =20A	-	30	-	S
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, F=1.0MHz	-	1900	-	PF
Output Capacitance	C <sub>OSS</sub>		-	130	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	95	-	PF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DS</sub> =30V, R <sub>L</sub> =1.5Ω V <sub>GS</sub> =10V, R <sub>G</sub> =3Ω	-	5	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	2.6	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	16.1	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	2.3	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =30V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V	-	30		nC
Gate-Source Charge	Q <sub>gs</sub>		-	4.5		nC
Gate-Drain Charge	Q <sub>gd</sub>		-	7.5		nC
Diode Forward Voltage <sup>(Note 3)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =30A	-		1.2	V
Diode Forward Current <sup>(Note 2)</sup>	I <sub>S</sub>		-	-	30	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> =20A di/dt = 100A/μs <sup>(Note3)</sup>	-	35	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	53	-	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

### Notes:

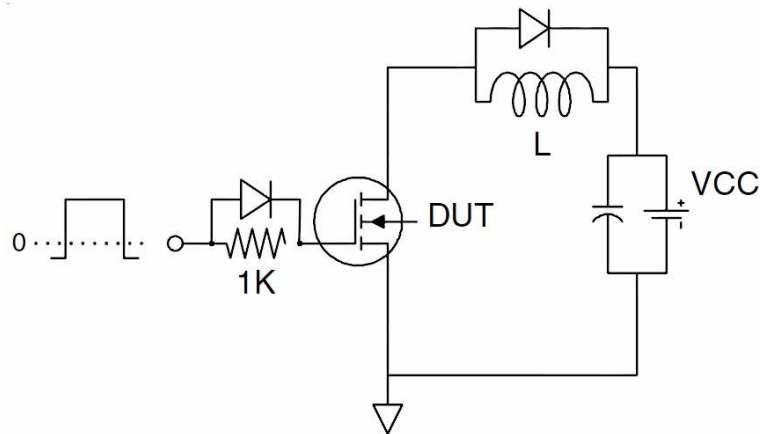
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition: T<sub>J</sub>=25°C, V<sub>DD</sub>=30V, V<sub>G</sub>=10V, L=0.5mH, R<sub>G</sub>=25Ω

## Test Circuit

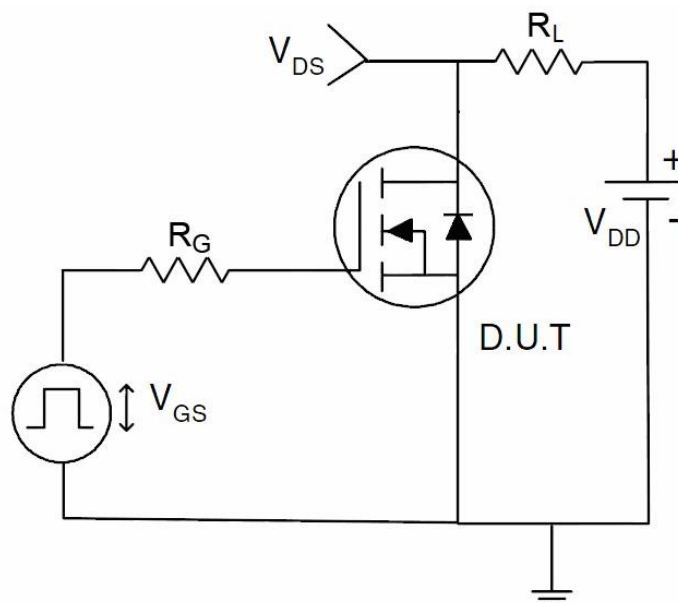
### 1) EAS test Circuit



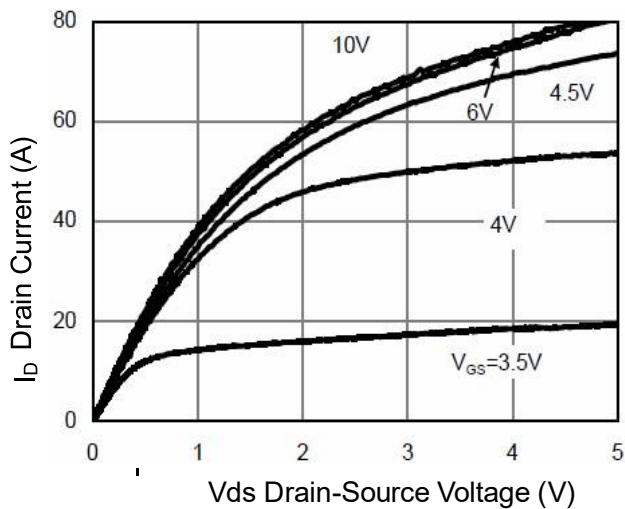
### 2) Gate charge test Circuit



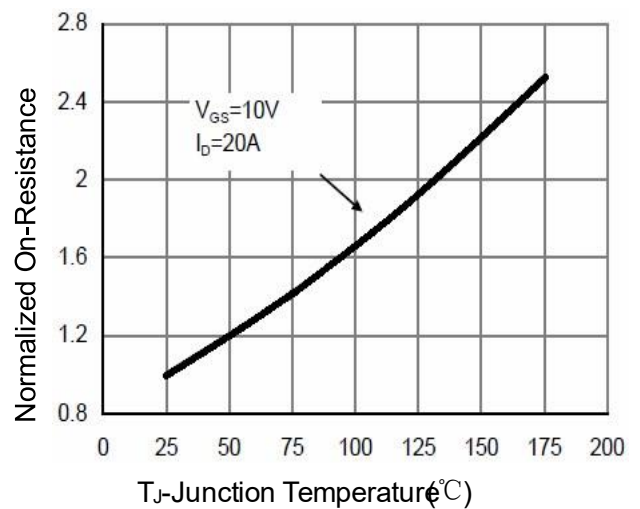
### 3) Switch Time Test Circuit



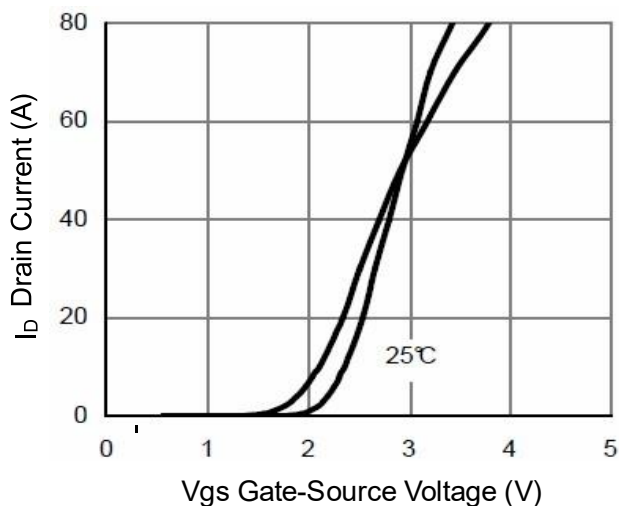
## Typical Electrical and Thermal Characteristics (Curves)



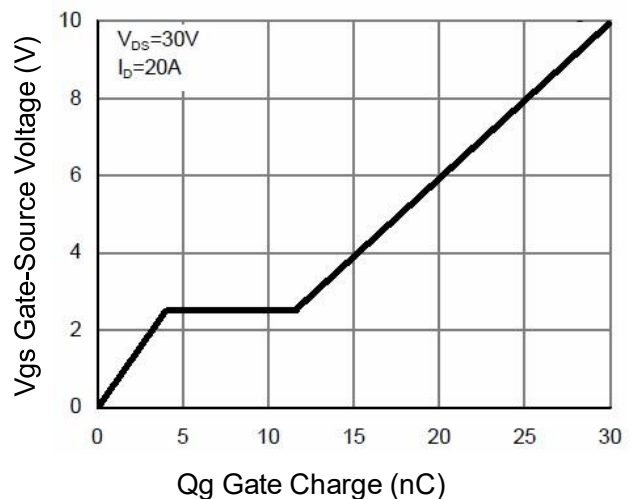
**Figure 1 Output Characteristics**



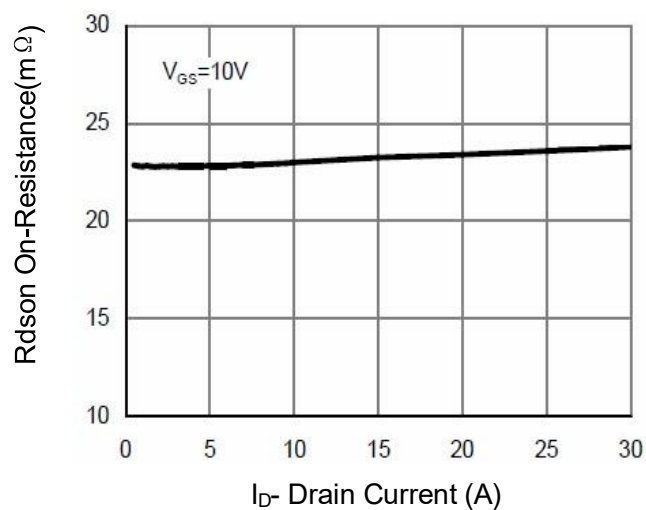
**Figure 4 Rds(on)-Junction Temperature**



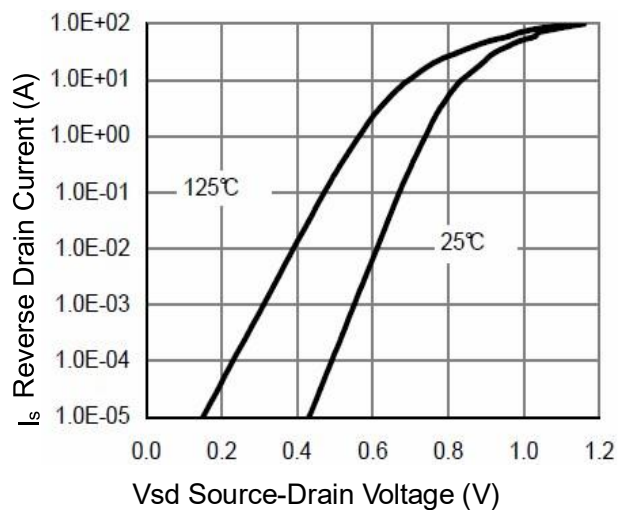
**Figure 2 Transfer Characteristics**



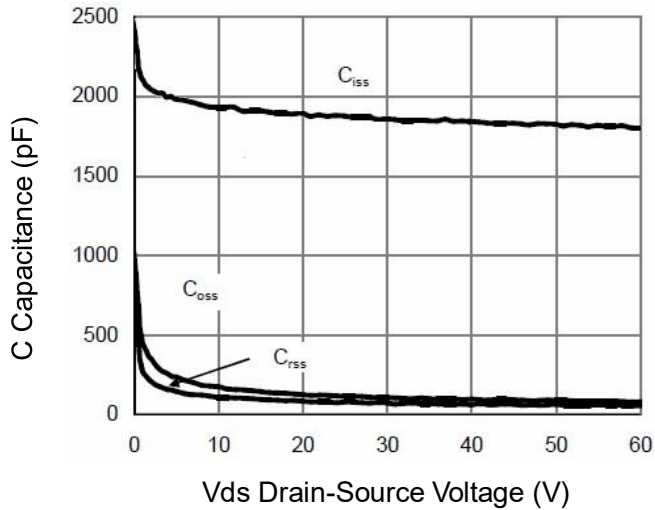
**Figure 5 Gate Charge**



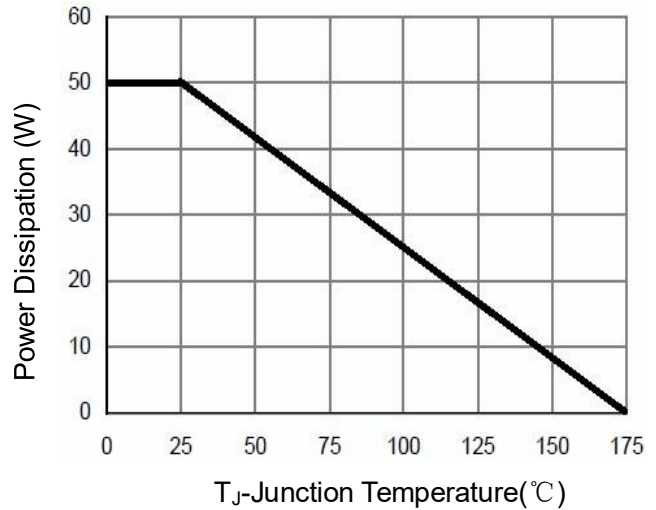
**Figure 3 Rds(on)-Drain Current**



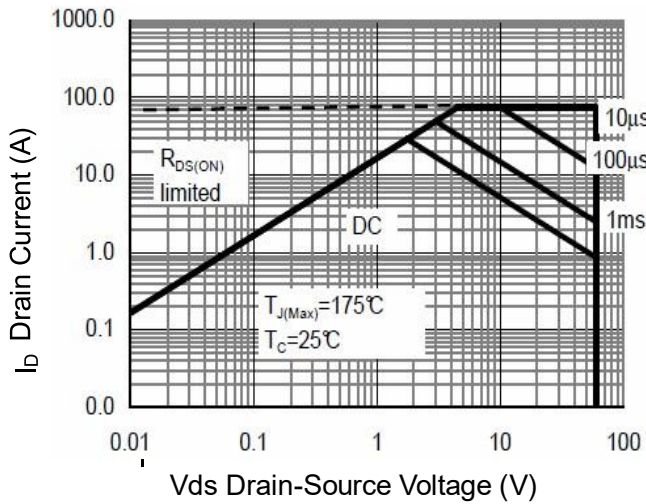
**Figure 6 Source-Drain Diode Forward**



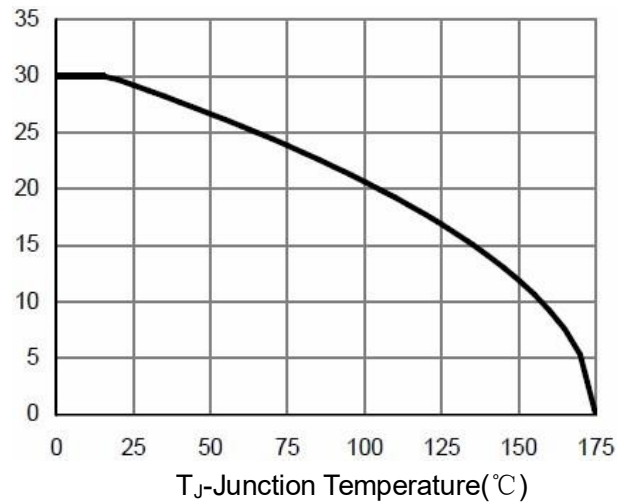
**Figure 7 Capacitance vs Vds**



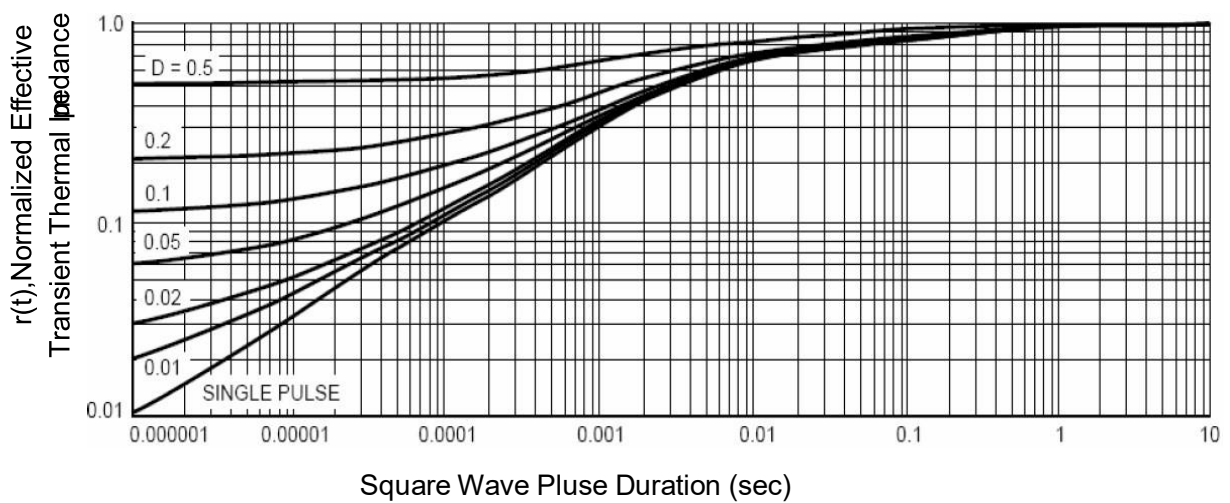
**Figure 9 Power De-rating**



**Figure 8 Safe Operation Area**

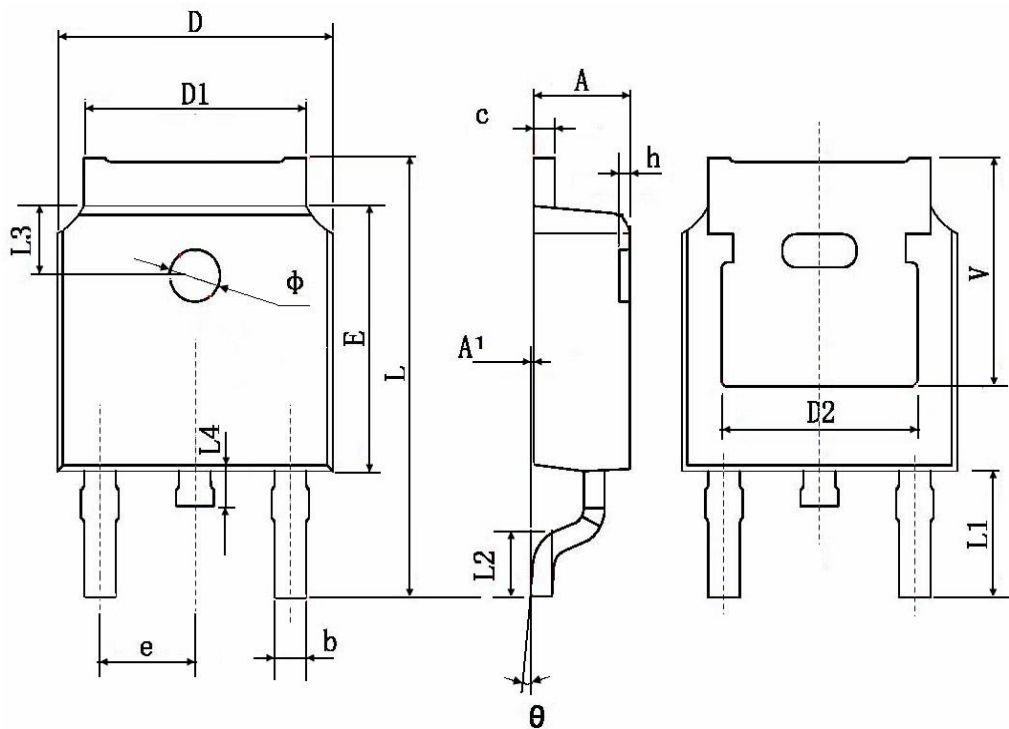


**Figure 10  $V_{GS(th)}$  vs Junction Temperature**



**Figure 11 Normalized Maximum Transient Thermal Impedance**

## TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	